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WHAT IS CLAIMED IS:

1. A circuit for distributing a clock signal having a clock frequency in an integrated circuit having a plurality of metal layers therein, comprising:

5 a capacitive clock distribution circuit having at least conductor therein; and
at least one inductor formed in a metal layer of the integrated circuit, each one
of said at least one inductor being coupled to said at least one conductor and having
an inductance value selected such that the at least one inductor and the capacitive
clock distribution circuit comprise a resonant circuit having a resonance frequency
10 substantially equal to the clock frequency.

2. The circuit for distributing a clock signal, as defined by claim 1, wherein the at
least one conductor in the clock distribution circuit includes a clock grid.

15 3. The circuit for distributing a clock signal, as defined by claim 2, wherein the at
least one conductor in the clock distribution circuit further includes a tree distribution
circuit coupled to the clock grid.

4. The circuit for distributing a clock signal, as defined by claim 3, wherein the
20 integrated circuit has a plurality of operating sectors and wherein the at least one
conductor further comprises a tree distribution circuit corresponding to a respective
one of the sectors of the integrated circuit.

5. The circuit for distributing a clock signal, as defined by claim 1, wherein the at
25 least one inductor includes a plurality of inductors distributed throughout the clock
distribution circuit.

6. The circuit for distributing a clock signal, as defined by claim 5, wherein the
plurality of inductors each take the form of a spiral inductor.

30 7. The circuit for distributing a clock signal, as defined by claim 6, further
comprising a plurality of decoupling capacitors formed in the integrated circuit, each
one of the plurality of decoupling capacitors corresponding to a respective one of the

plurality of spiral inductors, wherein each one of the spiral inductors is coupled to a power-ground grid potential in the integrated circuit by a corresponding decoupling capacitor.

- 5 8. The circuit for distributing a clock signal, as defined by claim 1, further comprising at least one decoupling capacitor formed in the integrated circuit, wherein the at least one inductor is coupled to a power-ground grid potential by the at least one decoupling capacitor formed in the integrated circuit.
- 10 9. A circuit for providing a clock signal in an integrated circuit comprising:
 a clock driver circuit, the clock driver circuit providing a clock signal having a clock frequency;
 a clock distribution circuit having at least one conductor therein, the clock distribution circuit being coupled to receive the clock signal from the clock
15 driver circuit; and
 a plurality of inductors coupled to the clock distribution circuit, the plurality of inductors being spatially distributed throughout the clock distribution circuit and having a total inductance value such that the inductors and the clock distribution circuit form a resonant circuit having a resonance frequency substantially
20 equal to the clock frequency.
10. The circuit for providing a clock signal, as defined by claim 9, wherein the at least one conductor in the clock distribution circuit includes a clock grid.
- 25 11. The circuit for providing a clock signal, as defined by claim 10, wherein the at least one conductor in the clock distribution circuit further includes a tree distribution circuit coupled to the clock grid.
- 30 12. The circuit for providing a clock signal, as defined by claim 11, wherein the integrated circuit has a plurality of operating sectors and wherein the at least one conductor further comprises a plurality of tree distribution circuits corresponding to respective ones of the plurality of operating sectors of the integrated circuit.
13. The circuit for providing a clock signal, as defined by claim 12, wherein the

clock driver circuit includes a plurality of buffer amplifiers, wherein each one of the plurality of tree distribution circuits corresponding to a respective one of the plurality of operating sector is coupled to at least one of the plurality of buffer amplifiers.

- 5 14. The circuit for a clock signal, as defined by claim 13, wherein the clock distribution circuit includes at least one further tree distribution circuit, said further tree distribution circuit being coupled to the buffer amplifiers in a plurality of sectors of the integrated circuit.
- 10 15. The circuit for providing a clock signal, as defined by claim 12, wherein the clock driver circuit comprises a plurality of phase lock loop circuits, wherein each one of the plurality of tree distribution circuits corresponding to a respective one of the plurality of operative sectors is coupled through the at least one of the plurality of buffer amplifiers to at least one of the plurality of phase lock loop circuits.
- 15 16. The circuit for providing a clock signal, as defined by claim 9, wherein each one of the plurality of inductors is a spiral inductor.
- 20 17. The circuit for providing a clock signal, as defined by claim 16, further comprising a plurality of decoupling capacitors formed in the integrated circuit, each one of the plurality of decoupling capacitors corresponding to a respective one of the plurality of spiral inductors, wherein the spiral inductors are coupled to a power-ground grid potential in the integrated circuit by a corresponding one of the plurality of decoupling capacitor.
- 25 18. The circuit for providing a clock signal, as defined by claim 17, wherein a voltage potential at a junction of one of the plurality of spiral inductors and a corresponding one of the plurality of the decoupling capacitors is provided as a reference voltage for pseudodifferential switching of the clock signal.
- 30 19. The circuit for providing a clock signal, as defined by claim 9, further comprising at least one capacitor switchably coupled to the clock distribution circuit, whereby the total capacitance of the clock distribution circuit can be tuned by switching said at least one capacitor.

20. A method of distributing a clock signal having a clock frequency in an integrated circuit having at least one clock distribution conductor therein, comprising:
- determining the capacitance of clock distribution conductor and circuitry coupled thereto;
- determining the inductance value of at least one parallel connected inductor required to form a resonance circuit with the clock distribution conductor and the circuitry coupled thereto, having a resonance frequency equal to the clock frequency; and
- coupling the at least one parallel-connected inductor to said clock distribution conductor to provide said inductance value.